CTμL 9953-9955 • 9964-9966 • 9971-9972 AND-OR GATES

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The Fairchild CTμL AND-OR gate is a PNP-NPN complementary logic circuit which provides the system designer with the basic tools for designing extremely fast, proven, low cost synchronous systems.

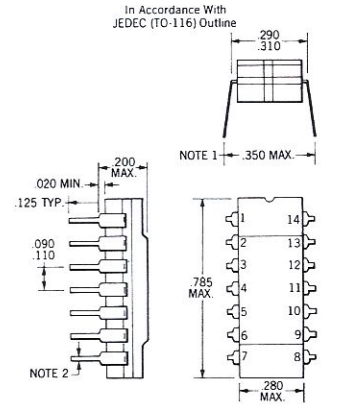
The following data, stressing worst case conditions, plus 100% testing by Fairchild for a minimum fanout of 11 and a maximum propagation delay of 4.5 nseconds at full fanout at 25°C, will assure the designer of proper worst case performance in his own system.

The AND-OR gate is basically a cascade connected PNP-NPN complementary non-saturating transistor pair. The output transistor is an emitter follower having virtually no threshold level. Therefore, there is no delay in output response due to input charging to threshold voltage, no stored charge to remove, negligible emitter-base transition charge and no collector-base transition capacity multiplication. Thus, typically 3 nseconds delays are obtainable at full fanout without the necessity of fast rise and fall time. This means conventional back panel wiring may be used with substantial reduction in inductive and capacitive noise usually generated by threshold circuits. The emitter follower low output impedance coupled with the high input impedance contributes to the large fanout and exceptional performance in the presence of stray capacitance.

CTμL circuits are packaged in the versatile JEDEC TO-116 DUAL-IN-LINE packages which are hermetically sealed ceramic units intended for low cost insertion techniques.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES:

- **Power supplies are 4.5 V ±10% and −2.0 V ±10%.**
- **High fanout capability**
- **Temperature range +15°C to +55°C**
- **Low power dissipation**
- **Low propagation delay — 3.0 ns typical**
- **Logic swing of 3.0 V**

PURCHASING INFORMATION:

Description	Code	Marking
CTμL9953 — 2-2-3 Input AND-OR Gate (three gates in one package)	U6A995379X	CTμL95379
CTμL9954 — Dual 4-Input AND-OR Gate (two gates in one package)	U6A995479X	CTμL95479
CTμL9955 — Dual Output 8-Input AND-OR Gate	U6A995579X	CTμL95579
CTμL9964 — 3-3-1 Input AND-OR Gate (three gates in one package)	U6A996479X	CTμL96479
CTμL9965 — Quad 1-Input AND-OR Gate	U6A996579X	CTμL96579
CTμL9966 — Quad 2-Input AND-OR Gate (with three outputs)	U6A996679X	CTμL96679
CTμL9971 — Quad 2-Input AND-OR Gate (with two outputs)	U6A997179X	CTμL97179
CTμL9972 — Quad 2-Input AND-OR Gate (with three outputs, all pull down resistors omitted)	U6A997279X	CTμL97279

Use the ten letter code for ordering purposes.
All units are marked as above unless otherwise specified.

*Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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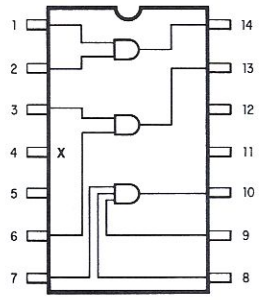
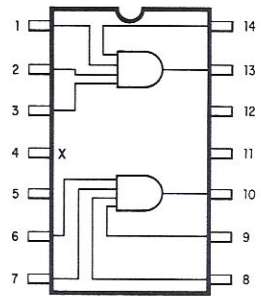
FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

PIN CONFIGURATION AND LOGIC DIAGRAM
(TOP VIEW)

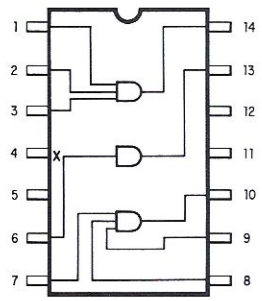
CTμL9953



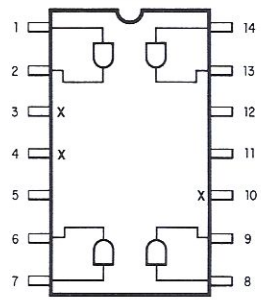
CTμL9954



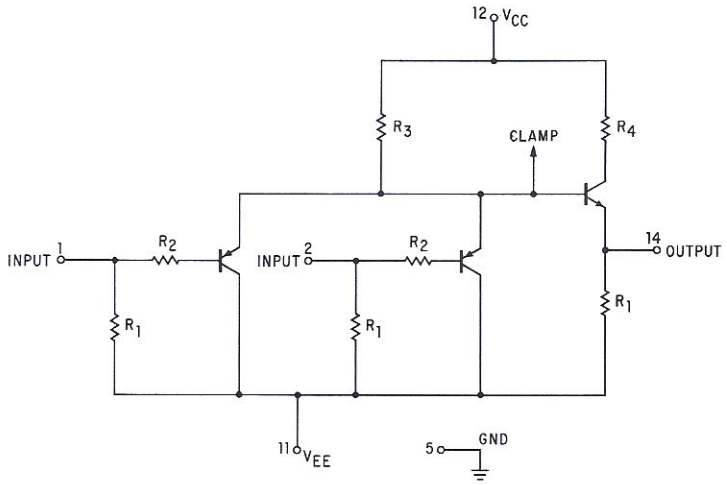
CTμL9964



CTμL9965

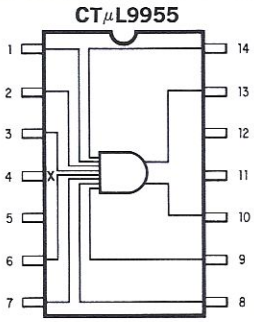


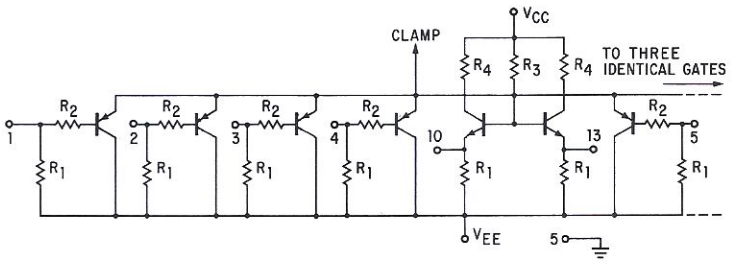
CIRCUIT DIAGRAM



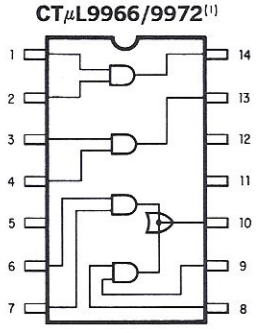
NOTE: Only one representative AND-OR gate shown.

CTμL9955

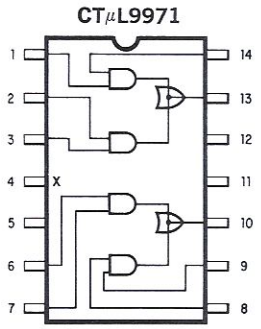


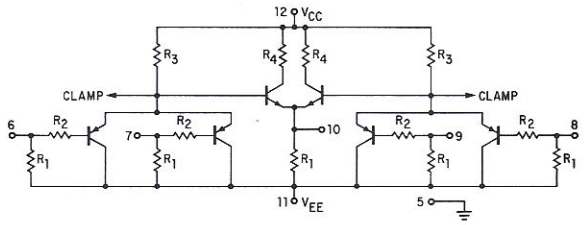


CTμL9966/9972[1]



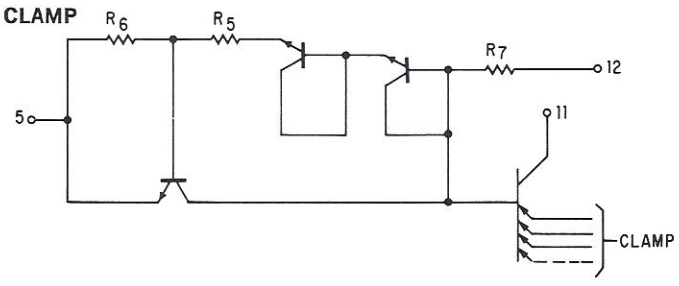
CTμL9971





NOTE: One AND/OR gate shown.

NOTES:
(1) R_1 deleted for CTμL 19972
X = Not connected.



Pin 12: $V_{CC} = 4.5\ V \pm 10\%$
Pin 11: $V_{EE} = -2.0\ V \pm 10\%$
Pin 5: Ground

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

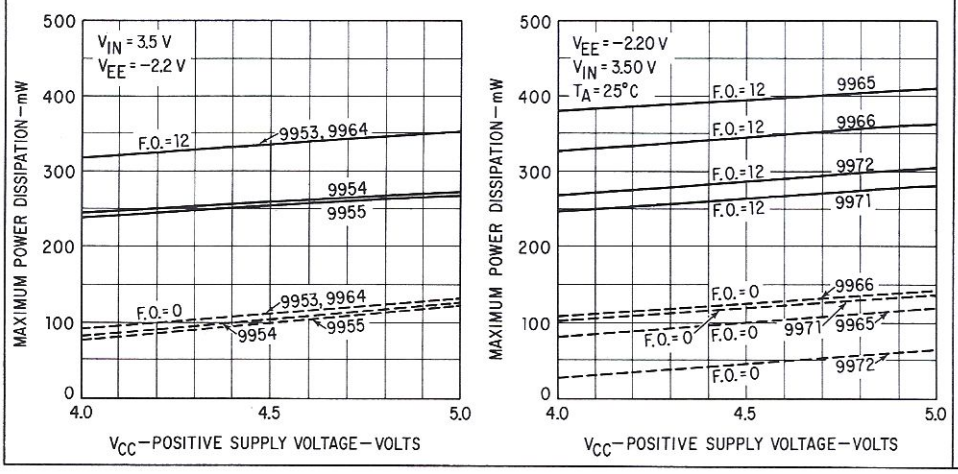
Maximum current in or out of a pin	100 mA	Maximum negative voltage applied to any input pin (output open)	−8.0 Volts
Maximum chip temperature	150°C	Maximum voltage applied to output pin (input grounded)	5.0 Volts
Maximum power dissipation	1.0 Watt		
Maximum voltage applied to any input pin	10 Volts		

D.C. TESTS

TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.(1)	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
ONE level offset		200	270	mV	4.05	−2.20	F.O. = 11(2)	Inputs sequentially to +2.25 V, other inputs to 3.5 V, pin 5 open. Worst case offset assuming ±10% supplies and W.C. parameters. Gates with lower input voltage will have smaller offsets; see fig. 12.
ZERO level offset		−120	−195	mV	4.95	−1.80	F.O. = 1	Worst case offset assuming ±10% supplies and min. fanout. Inputs sequentially to −0.36 V, other inputs to 3.50 V; pin 5 to GND.
Clamp level	2.10	2.30		Volts	4.05	−2.20	F.O. = 11	Inputs simultaneously at 3.5 V, pin 5 to GND. Tests minimum clamp level.
Clamp level		2.60	2.90	Volts	4.95	−1.80	No load	Inputs simultaneously to 3.5 V, pin 5 to GND. Tests max. possible clamp level to check existence of clamp.
Input resistors	1.6 k	2.0 k	2.4 k	Ω	4.05	−1.80	No load	Inputs to 3.5 V sequentially, other inputs to −0.7 V, sense input current. Tests min. R for max. loading, max. R for adequate turn-off and line termination.
Output resistors	1.6 k	2.0 k	2.4 k	Ω	4.05	−1.80	No load	Outputs to 3.5 V sequentially, inputs to −0.7 V, sense output current. Tests min. R for max. wired OR loading, max. R for adequate turn off.
Positive supply current, I_{PS}		I_{PS}	$I_{PS\ max}$	mA	4.95	−2.20	No load	Inputs to −0.7 V simultaneously.
Negative supply current, I_{NS}		$-I_{NS}$	$-I_{NS\ max}$	mA	4.95	−1.80	No load	Inputs to +3.5 V simultaneously.
Rising Propagation Delay, t_{dr}		3.5	4.5	ns	4.50	−2.00	F.O. = 12	See t_{pd} test circuit, page 6.
Falling Propagation Delay, t_{df}		3.0	4.0	ns	4.50	−2.00	F.O. = 12	See t_{pd} test circuit, page 6.

NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 11 equivalent to 145 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions

MAXIMUM POWER DISSIPATION VS. POSITIVE SUPPLY VOLTAGE

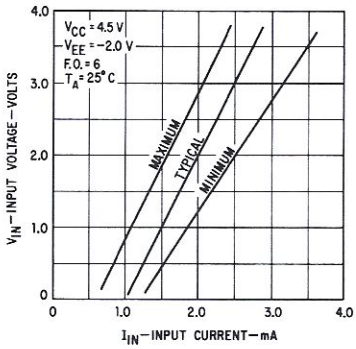


POSITIVE AND NEGATIVE CURRENT DRAIN

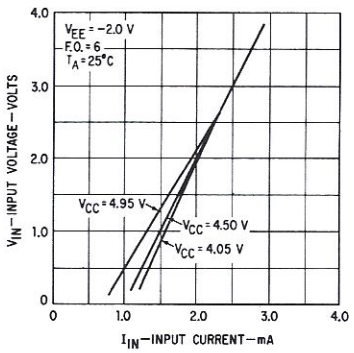
CTμL Element	$I_{PS\ typ}$	$I_{PS\ max}$	$I_{NS\ typ}$	$I_{NS\ max}$	UNITS
9953	22.0	27.7	33.0	41.4	mA
9954	16.5	20.5	33.0	39.6	mA
9955	11.5	14.3	30.0	37.1	mA
9964	22.0	27.7	33.0	41.4	mA
9965	28.0	34.9	29.0	36.0	mA
9966	27.0	33.9	38.0	47.5	mA
9971	26.0	32.9	36.0	44.6	mA
9972	12.0	20.0	5.0	10.0	mA

INPUT CHARACTERISTICS

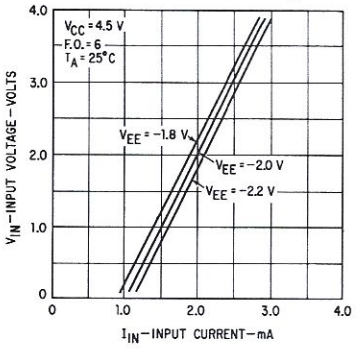
TOLERANCE VARIATION



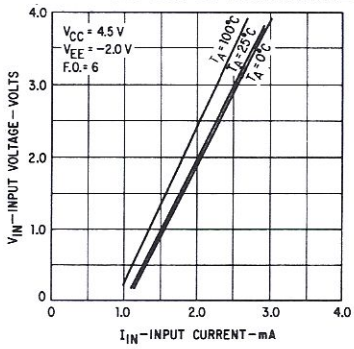
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF V_{EE}

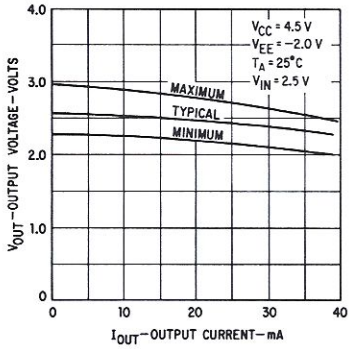


AS A FUNCTION OF TEMPERATURE

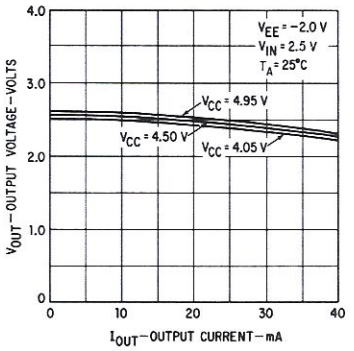


OUTPUT CHARACTERISTICS

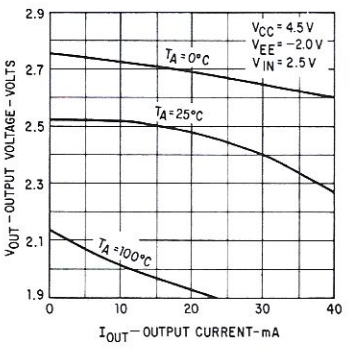
TOLERANCE VARIATION



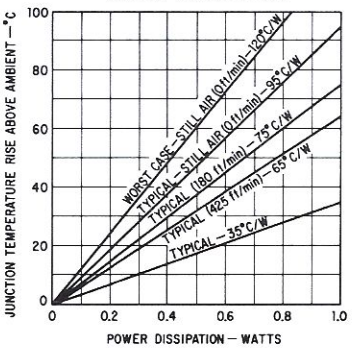
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF TEMPERATURE

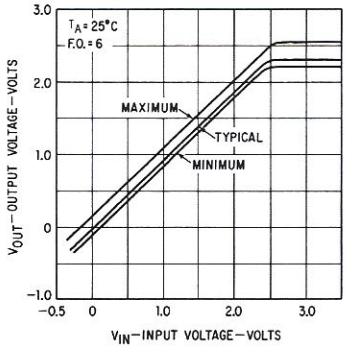


WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION

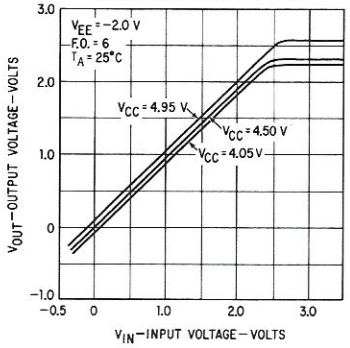

WORST CASE — STILL AIR (0 ft/min) — 120°C/W
TYPICAL — STILL AIR (0 ft/min) — 95°C/W
TYPICAL (180 ft/min) — 75°C/W
TYPICAL (425 ft/min) — 65°C/W
TYPICAL — 35°C/W
JUNCTION TEMPERATURE RISE ABOVE AMBIENT — °C
POWER DISSIPATION — WATTS

TRANSFER CHARACTERISTICS

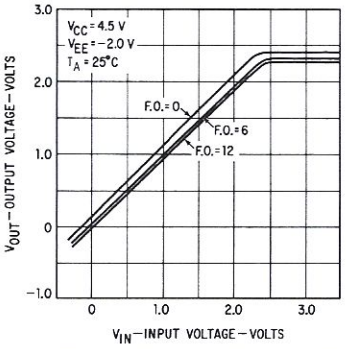
TOLERANCE VARIATION



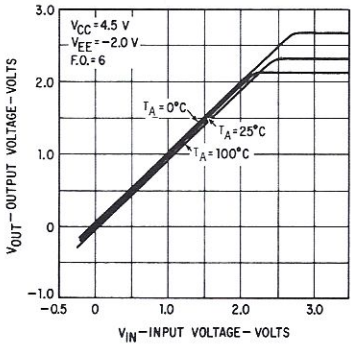
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF FAN OUT

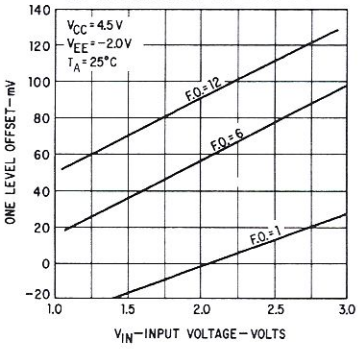


AS A FUNCTION OF TEMPERATURE

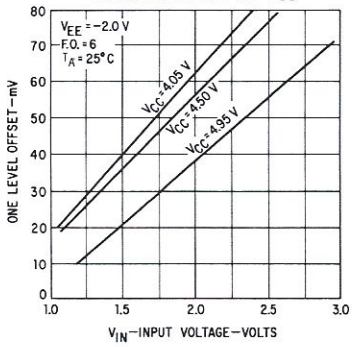


"ONE" LEVEL OFFSET

AS A FUNCTION OF FAN-OUT

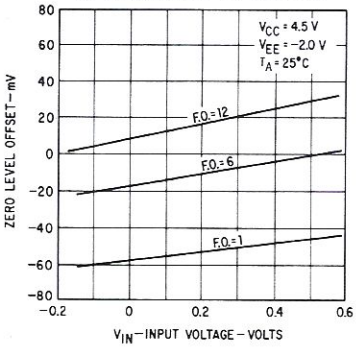


AS A FUNCTION OF V_{CC}

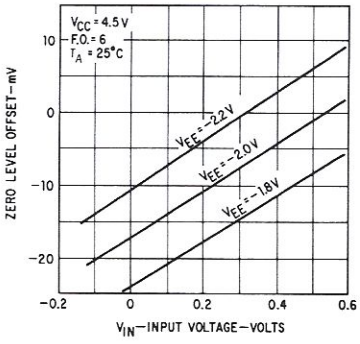


"ZERO" LEVEL OFFSET

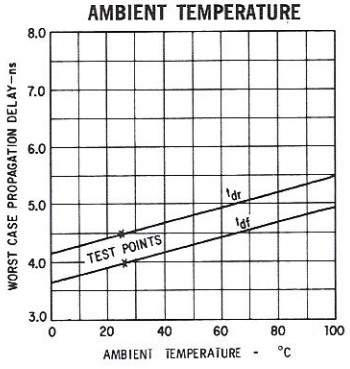
AS A FUNCTION OF FAN-OUT



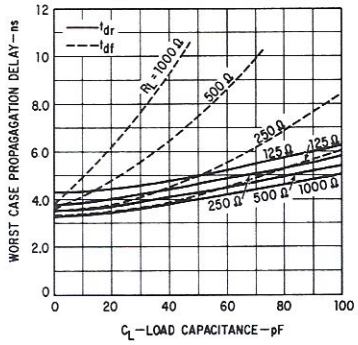
AS A FUNCTION OF V_{EE}



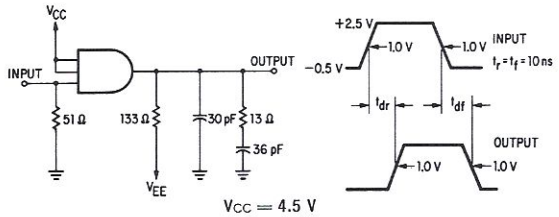
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



WORST CASE PROPAGATION DELAY VERSUS C_L AS A FUNCTION OF R_L

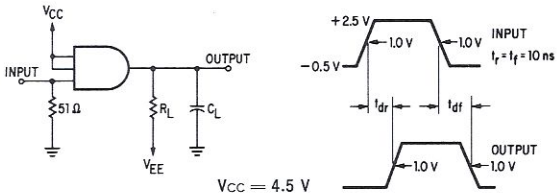


t_{PD} TEST CIRCUIT



$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

t_{PD} TEST CIRCUIT FOR ABOVE



$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

APPLICATION INFORMATION:

Greatest system speed will be realized by performing most of the logic with the use of the ultra-fast AND-OR gates. Consideration, however, must be given to level shifting, loading effects, impedance matching and ringing, which are inherent in fast switching systems. The AND-OR gates have built-in capability to overcome these problems. A few rules are outlined below to assist in solving these problems.

The electrical specification tests are performed under conditions chosen to emphasize the worst case results, and could be considered as conservative limits. For initial steps in designing new systems, typical values and data from graphs may be consulted for a realistic design. The different diagrams for each parameter are correlated through the nominal curve. To arrive at the worst case performance under a given set of conditions, deviation from nominal curve must be added or subtracted as the case may be.

INTERFACING — The AND-OR Gate should always be driven from another CTμL element. When interfacing from another logic form, or from a test signal generator, the signal should be introduced via a CTμL inverter, buffer, or flip-flop and then into the AND-OR Gate.

WIRED-OR — A powerful feature of the AND-OR Gates is that two or more outputs may be wired together to form the positive OR function at the output tie point, thus achieving two logic decisions in a maximum of 4.5 ns. Subtract 1 unit fanout for each OR added gate.

OFFSET LEVEL - NOISE IMMUNITY — The AND-OR Gate may be looked upon as a non-inverting amplifier having a gain of less than one. Thus, the output levels are offset from the input. The amount of offset is a function of loading, positive and negative power supplies, temperature, and input voltage and could be determined from the One and Zero level offset curves. When cascading AND-OR Gates, it should be noted that the offset of the first element has the largest offset and is decreasing sequentially on the following elements, due to smaller input level. It is recommended that noise-immunity levels be re-established by inserting such CTμL elements as the 952 Inverter, 956 Buffer, or 967 Flip-Flop after several offsets.

HIGH FREQUENCY RINGING — Each AND-OR Gate is internally equipped with a clamp circuit designed to reduce output ringing at high speed operation, at low fanout and moderate speed, the clamp may be released by leaving pin 5 open.

Any one length over 12″ long connected to the output should be terminated with a 200 Ω resistor to ground at the output. The 200 Ω approximates the characteristic impedance of back panel wiring. The 200 Ω termination is considered as a fanout of 4.

Regular equal spacing of AND-OR along a single path should be avoided as they tend to appear to the driving gate as a set of similarly tuned tank circuits and may induce ringing. When unavoidable, 200 Ω resistor to ground along the path will eliminate the ringing.

Large capacitive loads may cause ringing at the AND-OR Gate output and should be driven from a CTμL inverter or buffer.

UNUSED INPUTS — Unused inputs to the AND-OR Gate will effectively inhibit the gate output, and therefore, must be tied to the most positive voltage level. The unused input may be tied directly to $+V_{CC}$ or through a resistor not greater than 600 Ω. Unused inputs may be tied to active inputs at a cost of reduced fanout.

SHORT CIRCUIT PROTECTION — The AND-OR Gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground at V_{CC} not greater than 5 volts. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. Short circuiting the output to the —2 volts supply should be avoided.

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